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Original Paper

Erosion of stack current margin and voltage collapse boundary in a degrading shipboard DC distribution system with constant power loads

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Abstract: Stability assessment of constant power loads in shipboard direct-current (DC) distribution has fixed source parameters at beginning-of-life values, whereas the area-specific resistance (ASR) of a solid oxide fuel cell (SOFC) stack grows with operating time. For an SOFC–battery DC system with a stack current limit, the study establishes the degradation level at which a load step can no longer be absorbed and the time remaining before bus collapse. In an eleventh-order coupled model, the collapse boundary is the existence limit of a bus-voltage equilibrium with the stack at its current limit. For load steps of 1, 2 and 3 % it lies at ASR growth of 42.9, 29.5 and 16.1 %, and predicts every outcome of 45 transient cases. Beyond it the bus capacitance discharges against a net current deficit of a few amperes, so the collapse time follows from a quasi-static integral, accurate within 7 % away from the boundary and conservative near it, where it reaches 4.06 s. The time scales with bus capacitance, and battery droop moves the boundary to the combined stack–battery headroom. At a reference degradation rate the 2 % step capability is lost after 0.9 years and the static margin after 1.6 years.

Keywords: Solid oxide fuel cell, Shipboard direct-current distribution, Constant power load, Degradation, Voltage collapse, Bus capacitance

1. Introduction

Under the greenhouse-gas reduction strategy of the International Maritime Organization, the transition of shipboard power sources is progressing, and the solid oxide fuel cell (SOFC) is being considered as a candidate for auxiliary and propulsion power on account of its high electrical efficiency and fuel flexibility. Vessels adopting fuel cells as a primary source favor direct-current (DC) distribution over alternating-current distribution, and the architecture and stability of shipboard DC microgrids have accordingly received considerable attention **[1][2]**.

The central issue in the stability analysis of shipboard DC distribution is the constant power load (CPL). In modern shipboard DC microgrids, propulsion motors and hotel loads are supplied through tightly regulated point-of-load converters and therefore behave as CPLs, whose negative incremental impedance destabilizes the bus voltage **[3][4]**. Both small-signal and large-signal stability analyses are used to assess the influence of such loads **[1]**. Nonlinear control strategies proposed for stabilization include sliding-mode, synergetic, backstepping, model predictive, and passivity-based control **[3]**. Stabilization by linearization via state feedback has also been applied to shipboard medium-voltage DC systems **[5]**, and stability under droop control has been analyzed **[6]**.

Attempts have also been made to address uncertainty in the CPL. It has been pointed out that existing studies treat stability in the neighborhood of a particular equilibrium defined by the nominal load. In practice, however, the equilibrium of a direct-current microgrid depends on time-varying load conditions. This observation has been formulated as a robust stability problem for a polytopic uncertain linear system over a given load range **[7]**.

All such extensions, however, address uncertainty on the load side. The fact that source-side parameters vary with operating time, that is, that the source impedance is itself a function of degradation,

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has not been treated. An SOFC stack exhibits growth in area-specific resistance (ASR) with operating time, which lowers the stack voltage at a given current density.

This gap is evident in the recent literature. A study comparing SOFC and polymer electrolyte membrane fuel cells as auxiliary power for a 200 m bulk carrier is illustrative **[8]**. That study does not model fuel cell degradation explicitly as a time-dependent efficiency loss. Instead, degradation is reflected only indirectly, through an assumed stack lifetime of 40,000 h and an associated replacement interval. This illustrates that degradation is treated as a constant even in recent system-level assessments.

Conversely, research on SOFC degradation tends to terminate at the cell or stack level. Previous work likewise presented a durability prediction model under maritime environmental conditions and a hierarchical Bayesian reliability assessment based on a resistance growth law **[9][10][11]**. The outputs of that work were voltage trajectories, resistance values, and failure probabilities. What these quantities imply for the operation of a shipboard power system was not addressed. A separation therefore exists in which system analysis does not consider degradation and degradation research does not consider the system.

This study addresses this gap by coupling the electrochemical states of an SOFC stack and the states of the power conversion system into a single dynamic model, and by expressing the consequence of degradation in two quantities that a system designer can use. The first is the collapse boundary: the degradation level at which a given load step leaves no bus-voltage equilibrium with the stack at its current limit. The boundary is obtained from the full bus power balance, including the feeder loss and the voltage dependence of the hotel load, so that the static criterion and the transient response refer to the same quantity. The second is the time to collapse beyond the boundary, which determines the time available for load shedding; it is shown to follow from the discharge of the bus capacitance against the net current deficit and is therefore given in closed form. Small-signal eigenvalues are reported for the same conditions to confirm that the linearized model, which does not contain the current-limit inequality, cannot represent this risk. The results are obtained for a representative 5 MW system in which the battery is dispatched at constant power; the sensitivity of the boundary and of the time to collapse to battery droop participation, bus capacitance and feeder resistance is reported so that the design dependence of the quantitative results is explicit.

2. Analysis Method

2.1 System Configuration and Operating Conditions

The system under analysis is a shipboard DC distribution system comprising an SOFC stack, DC converters, a battery, a bus, and a CPL. This study does not address a specific vessel. Recent system-level assessments of marine SOFCs consider auxiliary power in the range of 360 to 600 kW for a 200 m bulk carrier **[8]**, whereas the present work assumes a stage at which the SOFC supplies part of the propulsion power and therefore adopts a system of approximately 5 MW. A DC microgrid of this type, with a fuel cell and a battery on a bus of about 1,000 V, has been operated in sea trials on a test vessel **[15]**.

The elementary unit of the degradation analysis, however, is the module rather than the system. The stack modeled here consists of ten modules of 328.6 kW each, and the output of a single module belongs to the same class as the approximately 400 kW unit adopted as the reference module in current marine SOFC demonstration programs **[11]**. This study therefore does not postulate an unproven large stack; it considers a system obtained by placing demonstration-scale modules in parallel. Because stack degradation is defined at the cell level, increasing the number of parallel modules does not alter the domain of validity of the degradation model. This scale was selected because the stack current limit constrains system behavior only when the SOFC supplies a substantial fraction of the load; here the SOFC supplies 3.29 MW of a total load of 5.0 MW.

The stack comprises ten modules, each of five parallel strings of 440 series-connected cells. With an active cell area of 360 cm^2 the total active area is 18,000 cm^2. The operating temperature is 750 °C, the rated current density is 0.45 A/cm^2, and the rated fuel utilization is 0.75. The rated current density defines the rated stack current of 8,100 A, and the stack current limit is set at 1.10 times this value, 8,910 A; the operating current density follows from the load and lies above the rated value at every operating point of this study (**Table 1**).

The nominal bus voltage is 1,000 V and the bus capacitance is 0.08 F. The SOFC converter employs droop control with a no-load setpoint of 1,000 V and a droop of 5 % referred to a rated current of 5,000 A. The bus voltage therefore varies with load, and its steady-state value at the reference load of this study is 966.7 V. Because this value is an operating point on the droop characteristic rather than a setpoint, all results below are interpreted as relative changes with respect to this operating point.

The load consists of a propulsion load of 4.0 MW and a hotel load of 1.0 MW. The propulsion load is supplied through a tightly regulated point-of-load converter and is therefore represented as a CPL, whereas the hotel load is represented by a constant-impedance, constant-current and constant-power model with shares of 0.3, 0.2 and 0.5. It has been noted that hotel loads in shipboard DC microgrids also behave as constant power loads **[3]**; the present model retains voltage-dependent components such as lighting and resistive heating. Because the constant-power share is 0.5, this setting is less severe for stability than treating the entire load as constant power. The bus and the load node are connected by a 60 m cable of 8.4 mΩ, which dissipates 241 kW, 4.8 % of the load, at the reference operating point; this value is retained as the reference case and a 1 mΩ feeder is examined in Section 3.6. The reference value corresponds to a single 240 mm² copper conductor pair over the 60 m run (loop length 120 m, resistivity 1.72×10^{-8} Ω·m) and therefore represents a long or lightly paralleled feeder; a feeder built from several parallel conductors, as is usual at this current, approaches the 1 mΩ case, so the two values bracket the practical range. The battery is represented by a two-branch resistor-capacitor equivalent circuit and supplies 2.0 MW in steady state, while the stack supplies 3.286 MW. In the reference condition the battery converter holds the terminal power at 2.0 MW, so the battery injects a constant power into the bus irrespective of the bus voltage; the dead-band droop characteristic of the battery converter is enabled in Section 3.6.

The following symbols are used throughout. The stack voltage and stack current are denoted v_{st} and i_{st}, the stack current limit I_{max}, the current density j, the fuel utilization U_f, the bus voltage v_S, and the stack power P_{stack}. The stack current margin is defined as $m = (I_{max} - i_{st})/I_{max}$.

2.2 Stack Polarization Model

The cell voltage is obtained by subtracting the ohmic loss, the activation overpotentials and the concentration overpotentials from the Nernst voltage, as given in **Equation (1)**.

$$V_{cell} = E - j\,R_{ohm} - \eta_{act,an} - \eta_{act,ca} - \eta_{conc} \tag{1}$$

Here E is the Nernst voltage, j the current density, R_{ohm} the ohmic ASR, and the remaining terms the activation and concentration overpotentials at the anode and cathode. The activation overpotentials are obtained as the numerical solution of the Butler–Volmer equation. The beginning-of-life (BoL) ASR is specified as 0.1764 Ω·cm², of which the ohmic component is 0.09654 Ω·cm² and the activation component is 0.07790 Ω·cm², with 28.6 % of the activation component assigned to the cathode.

This value is consistent with the BoL reference of 0.18 Ω·cm² adopted in degradation analyses of marine SOFCs **[11]**. The value is also not chosen independently of the stack configuration. Given an active area of 18,000 cm² and 440 series-connected cells, delivering the required output of 3.286 MW at the BoL operating current density of 0.465 A/cm² requires a cell voltage of the order of 0.89 V, which is satisfied by a resistance of 0.176 Ω·cm². The literature reference value and the design consistency requirement therefore indicate the same value.

The charge transfer coefficients and the exchange current densities are not specified directly but are obtained inversely from the resistances above. The reason is parameter consistency. The activation resistance is defined as the differential resistance of the Butler–Volmer equation and is therefore determined by the exchange current density and the charge transfer coefficient. If the activation resistance is specified as a design quantity while the other two are separately assigned literature values, the specifications will in general be mutually inconsistent and the model will fail to reproduce the specified resistance split. Only two of the three quantities may be assigned independently.

The resistance split is taken as the independent quantity in this work, because the manner in which degradation is distributed among the ohmic, activation and concentration components is the subject of the analysis in Section 2.3 and the split must therefore remain specifiable. The exchange current density and the charge transfer coefficient are consequently dependent quantities: the former is obtained so that the differential resistance at the rated operating point equals the specified activation resistance, and the latter is determined so that the overpotential distribution at the rated operating point is satisfied, giving 0.59 for the anode and 0.65 for the cathode. The two coefficients are thus derived rather than measured quantities.

2.3 Degradation Model

Degradation is represented as ASR growth. For a growth ratio relative to the BoL, the resistance increment is distributed among the ohmic, activation and concentration components. Because the distribution of degradation among these components depends on the stack design and the operating conditions, no particular distribution is assumed; six scenarios spanning the full range from purely ohmic

to purely activation degradation were analyzed, and the dependence of the results on the distribution is presented in Section 3.1.

The principal analysis in this paper takes the purely ohmic scenario A as the reference. Among the scenarios it has the highest critical degradation level, so the critical instants obtained on this basis are the latest ones that any distribution of the resistance increment can give, and the results for the other scenarios in Section 3.1 show how much earlier the critical instant falls when part of the increment is assigned to the activation and concentration components.

When converting degradation to operating time (Section 3.7), measured degradation rates reported in the literature are used. The reference value is 0.5 % per thousand hours, based on a stack operated for more than 93,000 h at 700 °C and 0.5 A/cm² **[12]**. The value of 0.6 % per thousand hours reported for a stack operated for 10,000 h **[13]** and a level of 1.0 % per thousand hours observed in the early period are given as upper bounds.

No dependence of the degradation rate on current density is introduced. This reflects long-term stack test results indicating that raising the current density and the fuel utilization does not fundamentally change the degradation rate, together with the observation that a higher voltage-referred degradation rate at higher current density may arise from the lower initial voltage **[13]**. The influence of operating parameters under accelerated test conditions has been reported separately **[14]**.

2.4 Coupled Model

The system model is implemented in the Modelica language and solved with OpenModelica **[16]**. Modelica supports acausal equation-based description, so the electrochemical state equations and the electrical circuit equations can be written at the same level without pre-assigning causality.

A boost converter is placed between the stack and the bus, and a bidirectional converter between the battery and the bus. Both converters are described by power-balance averaged models with an efficiency of 0.98 rather than by detailed switching models, since the time scale of interest is the transient response to a load step over a few hundred milliseconds. The results therefore depend on the current limit and the control bandwidths rather than on a particular circuit topology.

Control of the SOFC converter is a single loop in which a proportional-integral controller regulating the bus voltage generates a converter output current command, which is converted to a stack current command through the power balance. The voltage-loop bandwidth is 20 Hz, the current-loop bandwidth is 200 Hz, and the control bandwidth of the load converter is 100 Hz. The controller gains are 10.05 proportional and 729.4 integral, sized for a bus capacitance of 0.08 F. A preliminary analysis confirmed that the proportional gain must be adjusted together with any change of capacitance.

The essential nonlinear element of this study is the current command saturation. The current command generated by the controller is saturated at the stack current limit. The saturation is implemented as a smooth function of 25 A width, and the integral action of the voltage loop is inhibited while the saturation is active in order to prevent windup. In this state the converter no longer regulates the bus voltage, so the system behavior departs from the range predicted by the linearized model. This nonlinear constraint is central to the results of Section 3.

The battery is represented by a two-branch resistor-capacitor equivalent circuit with an open-circuit voltage of 716.3 V and a terminal current limit of 3,360 A. In the reference condition the battery converter holds the terminal power at 2.0 MW, so the battery current is constant at 3,005 A and the battery injects a constant power into the bus irrespective of the bus voltage. A dead-band droop characteristic, which raises the battery power by 78.8 kW per volt of bus-voltage deviation outside a ±4 V band, is implemented in the model and enabled only in Section 3.6.

The fuel system is modeled with a load-following fuel controller that saturates at the rated fuel flow. At all operating points of this study the stack current exceeds the rated current of 8,100 A, so the fuel flow is fixed at its rated value and the fuel utilization rises in proportion to the stack current; **Table 1** therefore corresponds to a fixed fuel flow.

The overall structure is shown in **Figure 1**, in which the bold block denotes the current command saturation linking the two subsystems, solid lines indicate power flow, and dashed lines measurement and control signals. The state variables were not selected arbitrarily; they are those for which differential equations remain after the governing equations of the components are assembled and the algebraic relations eliminated, and they number eleven. The electrochemical side comprises the drive power, the fuel utilization, four overpotentials and the stack current; the power conversion side comprises the two battery capacitor voltages, the bus voltage and the voltage-loop integrator state.

The eigenvalues of the system matrix linearized at the BoL equilibrium span approximately six orders of magnitude, from −0.0151 to −12,054. In view of this stiffness the integrator used is a differential algebraic system solver (DASSL in OpenModelica

1.27.0) with a relative tolerance of 1×10^{-8} and an output interval of 5 ms; the simulation is terminated by an event when the bus voltage reaches the feeder collapse limit defined in Section 2.5.

2.5 Analysis Procedure

In the static operating-point analysis, the stack operating point satisfying the constant power condition was obtained for each degradation level, and the current margin and the fuel utilization were evaluated. Under constant power operation the voltage drop is compensated by a rise in current, so the margin decreases as degradation proceeds.

In the collapse-boundary analysis, the existence of a saturated equilibrium after a load step is examined. With the stack at its current limit, the net current entering the bus capacitance is a function of the bus voltage alone, and a saturated equilibrium exists when this net current is non-negative at some bus voltage above the feeder collapse limit. The collapse boundary for a given step is the degradation level at which the maximum of the net current reaches zero; it is obtained by bisection on the ASR growth ratio. Because the net current is formed from the full bus power balance, including the feeder loss and the voltage dependence of the hotel load, the same balance governs the static criterion and the transient simulation. The expression is given in Section 3.4, **Equation (4)**.

In the linearization analysis, eleventh-order state-space models were extracted at the BoL and at 25 % resistance growth, and the eigenvalues, damping ratios and natural frequencies were compared.

In the transient analysis, 45 combinations of nine degradation levels and five load step sizes were analyzed, with the step applied at 0.1 s and the simulation run until the bus voltage either settled or reached the feeder collapse limit, with a horizon of 40 s. The parameters of each degradation level were pre-computed and applied by overriding them at run time; the parameters obtained in this way agree with those of an independently constructed reference case to within 0.004 % in every item.

Collapse is defined as the bus voltage v_S reaching the feeder collapse limit V_c, the lowest bus voltage at which the load-node equation $(v_S - v_B)/R_c = P/v_B + i_{ZIP}(v_B)$ has a solution; V_c is 394.5 V for the 2 % step. At this voltage the feeder current loses its solution and the simulation is terminated, and the time to collapse t_c is the instant at which it occurs. Transient results were classified into recovery to the pre-step bus voltage, settlement at a reduced bus voltage with the stack saturated, and collapse. Because the bus voltage falls steeply below about 700 V, the time at which it reaches V_c differs from the time at which it passes 400 V by less than 2 ms in every case.

The time to collapse is also estimated without simulation from the net bus current at the current limit, by integrating the discharge of the bus capacitance between the voltage at saturation and V_c; the expression is given in Section 3.5, **Equation (5)**, and compared there with the simulated times.

2.6 Simulation Environment and Verification

In computational analysis, model credibility is distinguished into verification and validation. Verification concerns whether the intended equations have been implemented without error, and validation concerns whether those equations correctly describe the physical phenomenon, established by comparison with measurement. What has been carried out in this work is verification; validation could not be performed as no measured data are available for comparison.

First, the governing equations are not newly proposed but are established formulations. The stack voltage follows the standard construction of the Nernst voltage less the ohmic loss, the Butler–Volmer activation overpotentials and the concentration overpotentials based on limiting current densities; the converters follow a power balance, the battery a two-branch resistor-capacitor representation, and the loads the standard constant-power and voltage-dependent representations.

Second, there are no free parameters. No coefficient has been adjusted to match a target result, and as described in Section 2.2 the charge transfer coefficients and exchange current densities are uniquely determined by the specified resistance split and the rated operating point. The possibility that the model has been tuned to produce a particular result is therefore excluded. That this construction satisfies the electrochemical relations was confirmed by a suite of 43 unit tests.

Third, the operating conditions and the degradation rate are anchored to external data. The BoL operating point is 750 °C, a current density of 0.465 A/cm², a fuel utilization of 0.776 and a cell voltage of 0.892 V, which lie within the operating range of long-term tests reported over more than 10,000 h **[13]**. The rate used in the conversion to operating time was likewise obtained from an operation of 93,000 h **[12]**. The conditions addressed by the model therefore lie in a region where measurements exist, and no

extrapolation is involved.

Fourth, two distinct implementations yield the same operating point. The static analysis solves the stack equations alone to obtain the current satisfying a given stack power. In the Modelica model, by contrast, the stack power is not supplied as an input; it emerges as a result of solving the power balance formed by the loads, the battery share, the converter efficiency, the cable loss and the bus voltage determined by the droop control. That the two paths agree at a stack current of 8,377 A and a bus voltage of 966.686 V indicates that the equations have not been corrupted in transcription and that the unit conversions and the power-balance accounting are consistent throughout.

What these four grounds establish, however, is the correctness of the implementation and the consistency of the steady state, not the quantitative accuracy of the transient response. The collapse trajectory following current command saturation has not been confirmed, as no measurements are available for comparison. Section 3.5 therefore separates the part of each collapse time that is fixed by the quasi-static bus balance from the part contributed by the transient drift of the stack voltage, and Section 4 states which of the results transfer beyond the parameter values of this system.

Static analysis alone, on the other hand, cannot yield the current command saturation, the discharge of the bus capacitance during saturation, or the time to collapse. These appear only in a coupled analysis in the time domain, which is the reason for constructing the Modelica model in addition to the static calculation. The complete set of 126 simulations reported in Sections 3.3 to 3.6 was reproduced with an independent transcription of the state equations in Python 3 (SciPy 1.18, LSODA, relative tolerance 1×10^{-8}); the outcome of every case was identical and the times to collapse agreed within 0.1 %. The parameter values and the state equations are listed in Appendix A.

3. Results

3.1 Erosion of the Current Margin by Degradation

Under constant power operation, a fall in stack voltage requires an increase in current to maintain the same output. The analysis below is carried out at a stack share of 3.286 MW and a current limit of 8,910 A. Although the bus voltage is determined by the droop control as a function of the converter output current, the steady-state bus voltage remains 966.686 V at all three degradation levels, so the change in current margin is attributable entirely to the voltage drop on the stack side. **Table 1** gives the steady-state operating points at three degradation levels.

A 50 % increase in resistance reduces the stack voltage by 5.90 % and raises the current by 6.27 %, so that the current margin is effectively exhausted, falling from 5.98 % to 0.08 %. The fuel utilization also rises from 0.776 to 0.824.

The following relation holds. Under constant power operation the current is the ratio of power to voltage, so the condition for the stack current to reach the limit is that the stack voltage falls below the critical value given in **Equation (2)**.

$$v_{crit} = P_{stack} / I_{max} = 3.286\ \text{MW} / 8{,}910\ \text{A} = 368.8\ \text{V} \quad (2)$$

This value corresponds to a loss of 5.981 % relative to the BoL voltage of 392.27 V, which is exactly equal to the BoL current margin. The relation of **Equation (3)** therefore holds.

$$\text{BoL current margin} = \text{tolerable stack voltage loss} \quad (3)$$

This relation permits the design margin to be converted directly into a tolerable stack voltage loss. The ASR growth that produces this loss depends on the distribution of the increment among the resistance components, as **Table 2** shows, so the operating time to the critical condition is evaluated on the ASR-growth axis for each scenario in Section 3.7.

Scenarios A and B are the two extremes of the distribution, and C, M and L are intermediate distributions with ohmic shares from 0.45 to 0.77. This range encompasses the spread of ohmic contributions reported for long-term stack operation **[12][13]**.

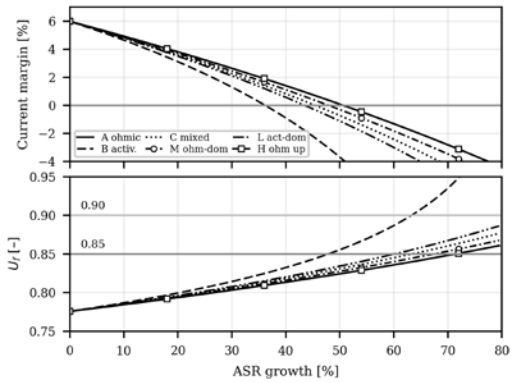


Figure 2: Stack current margin (upper) and fuel utilization (lower) as functions of resistance growth for five degradation distribution scenarios

Table 1: Steady-state operating points at three degradation levels

ASR gr. [%]	v_{st} [V]	i_{st} [A]	j [A/cm²]	U_f [–]	Margin [%]
0 (BoL)	392.27	8,377.3	0.4654	0.7757	5.98
25	381.12	8,622.3	0.4790	0.7983	3.23
50	369.11	8,902.7	0.4946	0.8243	0.08

Table 2: Degradation distribution scenarios and critical resistance growth ratios

Scenario	Ohmic:activ.:conc.	Zero m. [%]	U_f = 0.85 [%]	First limit
A ohmic (ref.)	1.00:0:0	50.60	71.39	Current
B activation	0:1.00:0	36.15	47.85	Current
C balanced	0.45:0.42:0.13	45.42	63.37	Current
M ohmic dom.	0.77:0.23:0	47.90	67.40	Current
L activ. dom.	0.47:0.53:0	43.48	60.13	Current

Table 3: Eigenvalues of the eleventh-order coupled model

No.	BoL [1/s]	ASR +25 % [1/s]	Change
1	−0.015144	−0.015144	0.00 %
2	−0.19569	−0.19569	0.00 %
3	−1.8452	−1.8311	−0.77 %
4	−2.0728	−2.0728	0.00 %
5, 6	−39.902 ± j83.340	−39.851 ± j83.466	–
7	−48.9997	−48.9989	0.00 %
8	−325.87	−327.05	+0.36 %
9	−627.84	−627.84	0.00 %
10	−1,199.47	−1,160.19	−3.27 %
11	−12,053.9	−12,122.2	+0.57 %

The upper panel of **Figure 2** shows the reduction of the current margin as resistance grows. All five curves start from the BoL value of 5.98 % and decrease monotonically, and the point at which each crosses the zero-margin line is the critical degradation level for that distribution. The curves separate because, for the same resistance growth, the resulting voltage loss depends on the component affected. The activation resistance is nonlinear in current density, so a given resistance increase produces a larger voltage loss, and the purely activation case therefore crosses zero furthest to the left. The two extremes differ by 14.45 percentage points.

The lower panel shows the corresponding rise in fuel utilization. Under constant power operation an increase in current raises the fuel consumption, and the fuel utilization rises even though the fuel supply is controlled proportionally to the current. The two horizontal lines mark the conventional design limit of 0.85 and the fuel starvation limit of 0.90. All five curves reach the 0.85 line only after crossing zero margin in the upper panel. The current limit is therefore always reached first, and this conclusion does not depend on the assumed distribution. The critical degradation level lies between 36.15 % and 50.60 %.

3.2 Small-Signal Stability Analysis

Eleventh-order state-space models were extracted at the BoL and at 25 % ASR growth and their eigenvalues compared. All eleven eigenvalues are listed in **Table 3**; the complex conjugate pair is given as a single entry.

All eleven eigenvalues lie in the left half-plane in both conditions. Of the eleven, seven move between the BoL and 25 % resistance growth and four are unchanged to five significant figures: the two slowest eigenvalues at −0.015144 and −0.19569 1/s, associated with the battery capacitor branches, the anode gas-diffusion mode at −2.0728 1/s, which equals its corner frequency of $2\pi \times 0.33$ Hz, and the load-converter pole at −627.84 1/s, which is set by the drive bandwidth and is independent of the stack. Of the seven that move, six shift by less than 1 %. The largest shift is in the eigenvalue at −1,199 1/s, which moves to −1,160 1/s (3.27 %, towards the imaginary axis) in a fast mode whose time constant of 0.83 ms is far shorter than the time scale of interest, while the eigenvalues at −325.9 and −12,054 1/s move away from the axis. The stability margin is altered by degradation by less than 4 %.

The complex conjugate pair merits closer attention because it governs the damped response to a load step. Its damping ratio falls from 0.4318 to 0.4309, a reduction of 0.2 %, and its natural frequency rises from 14.706 Hz to 14.720 Hz. Neither change would be detected in practice.

The linearized model is formed at the unsaturated operating point and does not contain the inequality $i_{st} \le I_{max}$, so the distance between the operating point and the current limit cannot appear in the eigenvalues; this is a known property of small-signal criteria rather than a result of this study. Under the same condition the stack current has already reached 96.8 % of the limit, which motivates the boundary and time-domain analyses that follow.

3.3 Transient Response to Load Steps

Transient analyses were performed for 45 combinations of nine degradation levels and five load step sizes. **Table 4** gives the outcome of each case as the time to collapse, with R denoting recovery to the pre-step bus voltage and S denoting settlement at a reduced bus voltage with the stack saturated. Every entry is monotonic in both the degradation level and the step size.

Three outcomes occurred. In the recovery cases the stack current remained below the limit, or touched it transiently as at 25 % growth with the 2 % step, and the bus voltage returned to its pre-step value. In the single settlement case, 40 % growth with the 1 % step, the stack current saturated and the bus voltage settled at 936 V without recovering, because the reduced voltage lowered the constant-impedance and constant-current parts of the hotel load enough to balance the bus. In all other cases the bus voltage declined after

saturation and reached V_c at the times listed. The first collapsing entry of each column shows the strongest dependence on degradation: for the 2 % step the time to collapse fell from 4.06 s at 30 % growth to 0.91 s at 35 %, 0.57 s at 40 % and 0.37 s at 50 %. A +10 % step cannot be tolerated even in the new condition, and a +5 % step collapses at the BoL after 0.62 s.

Figure 3 shows the case at 30 % growth with the 2 % step. The stack current reached the limit 20 ms after the step and remained there. The battery current stayed at 3,005 A throughout, as required by constant-power dispatch. The net current into the bus capacitance was about −9 A immediately after saturation, rose to about −2 A between 1.5 and 2.5 s while the bus voltage passed through 860–880 V, and then grew in magnitude as the bus voltage fell, reaching V_c at 4.06 s. The bus voltage therefore declined at a rate set by the small net current deficit and the 0.08 F bus capacitance, and the deferral of collapse is the passage of the bus voltage through the region in which the deficit is smallest.

3.4 Collapse Boundary

With the stack at its current limit I_{max}, the net current entering the bus capacitance is a function of the bus voltage alone,

$$i_{net}(v_S) = \eta\, v_{st}(I_{max})\, I_{max} / v_S + \eta\, v_{bt}\, i_{bt} / v_S - i_c(v_S) \qquad (4)$$

where $v_{st}(I_{max})$ is the steady stack voltage at the current limit for the degradation level considered, i_{bt} and v_{bt} are the battery current and terminal voltage, η the converter efficiency, and $i_c(v_S)$ the feeder current obtained from the load-node equation of Section 2.5, which exists only for bus voltages above V_c. A saturated equilibrium exists when $i_{net}(v_S) \geq 0$ for some v_S in (V_c, V_{nom}], and the collapse boundary for a given step is the degradation level at which the maximum of i_{net} over this interval reaches zero.

Figure 4 shows the net bus current of **Equation (4)** as a function of bus voltage for the 2 % step at 25, 30 and 35 % growth. At 25 % growth the curve crosses zero at 775 and 961 V, so a saturated equilibrium exists and the simulated bus voltage recovered to 960 V. At 30 % growth the maximum of the curve is −1.9 A at 861 V: no equilibrium exists, and the small magnitude of the deficit at the maximum is the origin of the 4.06 s deferral. At 35 % growth the maximum is −21 A and collapse followed within 0.9 s. The shape of the curves follows from the three terms of Equation (4): the stack and battery terms grow as $1/v_S$ when the bus voltage falls, whereas the feeder current grows faster because the CPL current rises as $1/v_B$ and the feeder loss as i_c^2, so the net current has an interior maximum and the feeder collapse limit at V_c.

Table 4: Time to collapse t_c [s] for nine degradation levels and five load steps (R: recovery; S: saturated settlement at 936 V; *: current limit reached transiently)

ASR growth	+1 %	+2 %	+3 %	+5 %	+10 %
0 %	R	R	R	0.622	0.187
10 %	R	R	R	0.382	0.179
20 %	R	R	1.242	0.298	0.172
25 %	R	R*	0.670	0.274	0.169
30 %	R	4.055	0.486	0.255	0.166
35 %	R	0.906	0.396	0.240	0.164
40 %	S	0.573	0.341	0.228	0.161
45 %	1.613	0.441	0.305	0.218	0.159
50 %	0.712	0.369	0.278	0.209	0.157

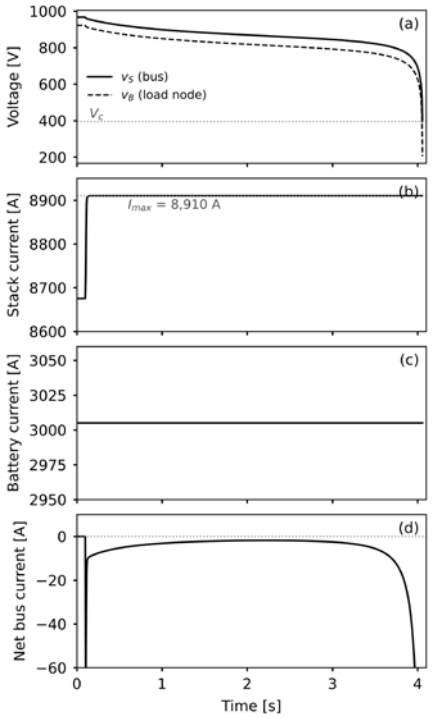


Figure 3: Bus and load-node voltages, stack current, battery current and net bus current for a +2 % load step at 30 % ASR growth

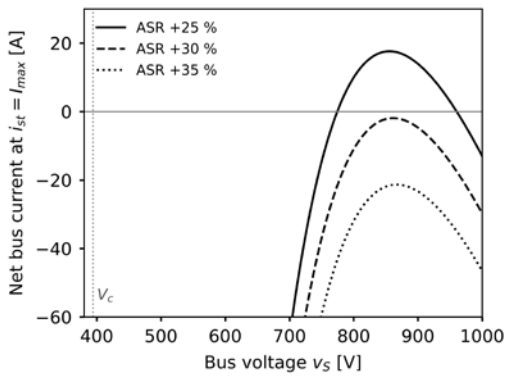


Figure 4: Net bus current at the stack current limit as a function of bus voltage for a +2 % load step at 25, 30 and 35 % ASR growth

Table 5: Collapse boundary from **Equation (4)** and transient outcome (a negative boundary means that no saturated equilibrium exists even at the BoL, so the step cannot be absorbed by the undegraded system)

Load step	Boundary ASR growth [%]	Bus voltage at boundary [V]	Highest recovering level [%]	Lowest collapsing level [%]
+1 %	42.9	857	40 (settled)	45
+2 %	29.5	861	25	30
+3 %	16.1	865	10	20
+5 %	−10.8	873	–	0
+10 %	none	–	–	0

Table 5 lists the boundary for each step size. The boundary lies inside the interval between the highest recovering and the lowest collapsing level of Table 4 for every step size, and for the 5 % step it lies below the BoL, consistent with the collapse of the BoL system under that step. The equilibrium bus voltage at the boundary, 857–873 V, is the voltage at which the simulated trajectories of the near-boundary cases lingered. The current margin of Section 3.1, which is defined at the pre-step operating point, and the boundary of **Table 5** are related through the step size: a system that retains a margin of 2.63 % at 30 % growth has lost the 2 % step capability because the stack voltage falls as the current rises and, at the reduced bus voltage that follows saturation, the feeder loss and the CPL current both increase, so that the stack current required to absorb the step exceeds the pre-step margin.

3.5 Time to Collapse

After the current command saturates at the instant t_{sat}, the stack current is fixed at I_{max} and the bus voltage obeys $C_{bus}\,\mathrm{d}v_S/\mathrm{d}t = i_{net}(v_S)$, so that the time to collapse follows from **Equation (4)** as

$$t_c - t_{sat} = C_{bus} \int \mathrm{d}v \,/\, [-i_{net}(v)], \quad \text{from } V_c \text{ to } v_S(t_{sat}) \tag{5}$$

which is evaluated with $v_{st}(I_{max})$ taken as the steady stack voltage at the current limit. **Figure 5** compares the simulated time to collapse with **Equation (5)** for all collapsing cases. For cases at least five percentage points beyond the boundary the integral reproduces the simulation within 1 to 7 %; for the three cases closest to the boundary (30 % growth with the 2 % step, 20 % with the 3 % step and the BoL with the 5 % step) it underestimates the time by 12 to 17 %, because the stack voltage at the current limit continued to fall during the slow passage as the fuel utilization and the diffusion overpotentials

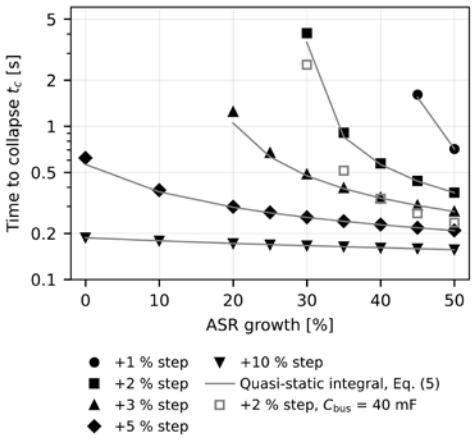


Figure 5: Simulated time to collapse and the quasi-static estimate of **Equation (5)** as functions of ASR growth for each load step, and for the +2 % step also with the bus capacitance halved to 40 mF

relaxed, which the single steady value of $v_{st}(I_{max})$ in **Equation (5)** does not include. The estimate is therefore conservative where the time to collapse is longest.

Equation (5) is linear in the bus capacitance for a given net-current curve. With the capacitance halved to 40 mF the simulated interval between saturation and collapse was 0.46 to 0.50 times the reference value for all cases at least five points beyond the boundary, and 0.54 and 0.61 times for the two cases closest to it (20 % growth with the 3 % step and 30 % growth with the 2 % step), where the stack-voltage drift adds a component that does not scale with capacitance. The boundary itself did not change, since **Equation (4)** does not contain the capacitance. The bus capacitance therefore sets the time available for a corrective action without altering the degradation level at which the action becomes necessary.

3.6 Battery Droop Participation and Feeder Resistance

With the dead-band droop of the battery converter enabled at 5 %, no collapse occurred for steps up to 5 % at any degradation level: the battery current rose from 3,005 A to between 3,017 and 3,337 A and the minimum bus voltage within the 40 s horizon of Section 2.5 was 961 V. At 50 % growth with the 5 % step the battery reached its current limit of 3,360 A and the bus voltage then declined slowly. This run was extended beyond the 40 s horizon of Section 2.5 to 600 s; the bus voltage passed 949 V at 120 s and settled at 943 V, below that minimum, which is the saturated equilibrium given by **Equation (4)** with both sources at their limits (zero crossing at 944 V), so the case is a settlement at reduced voltage rather than a collapse. All other droop-enabled runs used the 40 s horizon. Collapse occurred

only for the 10 % step, after the battery had reached its limit, with times from 0.56 s at the BoL to 0.20 s at 50 % growth. After the battery saturates the outcome is again decided by **Equation (4)** with the battery term fixed at its limit: for the 5 % step an equilibrium exists at every degradation level examined, whereas for the 10 % step the maximum of the net current is negative at every level and the bus collapses. The collapse boundary in this mode is set by the sum of the stack and battery current headroom; stack degradation consumes the stack share of that headroom, and the boundary of **Table 5** is recovered when the battery share is zero. The quantitative results of Sections 3.3 to 3.5 therefore apply to the operating mode in which the battery is dispatched at constant power, as during state-of-charge management, and are conservative for the mode in which it participates in voltage regulation.

With the feeder resistance reduced from 8.4 to 1 mΩ the BoL current margin rose from 5.98 to 12.0 %, the margin at 50 % growth was 7.3 %, and no collapse occurred for the 2 and 3 % steps up to 50 % growth. The erosion of the margin by degradation, 10.5 A of stack current per percentage point of ASR growth with the 8.4 mΩ feeder and 8.4 A with the 1 mΩ feeder, is of the same order in both cases; what the feeder resistance changes mainly is the headroom from which that erosion is subtracted. The degradation level at which a step capability is lost is therefore a function of the design headroom, and the values of **Table 5** are those of a stack sized at 1.10 times its rated current behind a feeder dissipating 4.8 % of the load.

3.7 Conversion to Operating Time

The degradation levels of **Table 5** are converted to operating time with the reference voltage degradation rate of 0.5 % per thousand hours measured at constant current density **[12]** and an annual operation of 6,000 h. At constant current density the voltage loss equals the current density times the ASR growth. The conversion is made at the BoL operating point of Table 1, a cell voltage of 0.892 V (the stack voltage of 392.27 V divided by the 440 series-connected cells) at a current density of 0.465 A/cm², so that the voltage and the current density belong to the same operating point; the rated current density of 0.45 A/cm² of Section 2.1 is the design quantity that defines the rated stack current. At this point the rate corresponds to an ASR growth of 0.0096 Ω·cm² per thousand hours, 5.4 % of the BoL value, and the ASR growth ratio increases linearly with operating time. The rate of **[12]** was measured at 700 °C, 50 K below the operating temperature of the model; the temperature enters the BoL resistance of Section 2.2, and no separate temperature correction is applied to the growth rate, which is used as the reference value of Section 2.3 with the higher rates quoted there as upper bounds. The conversion is applied to the ASR growth itself, so it is independent of the operating mode in which the degradation is observed, and the scenarios of **Table 2** give different operating times through their different critical growth ratios. **Table 6** gives the result for the reference scenario A.

Table 6: Operating time to each boundary at the reference degradation rate (scenario A, 6,000 h per year)

Condition	ASR growth [%]	Operating hours	Years
Loss of 3 % step capability	16.1	2,970	0.49
Loss of 2 % step capability	29.5	5,430	0.91
Loss of 1 % step capability	42.9	7,900	1.32
Exhaustion of static margin	50.6	9,320	1.55

At the reference rate the 2 % step capability is lost after 0.91 years while the static margin lasts 1.55 years, and the 3 % step capability after 0.49 years. These values are estimates for the assumed reference condition; a degradation rate twice the reference value halves them, and the ratio between the loss of the 2 % step capability and the exhaustion of the static margin, 0.58, is independent of the rate. The corresponding point lies at less than 25 % of the 40,000 h stack lifetime commonly assumed in system-level assessments **[8]**.

4. Discussion

The results connect three quantities that have been treated separately in shipboard DC studies: the small-signal stability of the regulated system, the stack current limit as a design margin, and the degradation of the source. The eigenvalue analysis confirms that the first is insensitive to degradation, and Section 3.1 shows that the second is consumed linearly. The contribution of the present work lies in the boundary of **Equation (4)** and the time of **Equation (5)**, which translate the consumed margin into the two quantities a designer needs: the degradation level at which a given load step can no longer be absorbed, and the time that remains before the bus collapses once it cannot.

The boundary is a static quantity, but it must be evaluated from the full bus balance. A stack-only balance, which assigns the step to the stack power alone, places the 2 % boundary at about 31 % growth, whereas the full balance places it at 29.5 %; the difference is the additional stack current demanded by the feeder loss and by the CPL

at the reduced bus voltage that follows saturation. The transient overshoot of the stack current does not determine the outcome: at 25 % growth the current touched the limit and the system recovered, because an equilibrium existed. What the overshoot determines is whether saturation is entered, and once it is entered the outcome is fixed by the sign of the maximum of **Equation (4)**.

The deferral of collapse, which reaches 4 s at the boundary, is the slow passage of the bus voltage through the region where the net current deficit is smallest, and it is sustained by the bus capacitance. Two consequences follow for design. First, the time available for automatic load shedding is proportional to the bus capacitance, so the capacitance can be specified against a required reaction time once the degradation level and the step size are given. Second, a battery that participates in voltage regulation moves the boundary to the combined current headroom, so that the degradation level at which the stack share is exhausted becomes the point at which the battery share begins to be consumed rather than the point of collapse. The quantitative values depend on the feeder loss and on the stack sizing margin, as Section 3.6 shows, and the method of Sections 2.5, 3.4 and 3.5 is intended to be applied to a given design rather than the values of **Table 5** to be transferred.

The analysis is based on averaged converter models, which omit switching-frequency ripple and the thermal limits of the semiconductor devices; both act on time scales shorter than the hundreds of milliseconds to seconds over which the collapse develops, and the current limit I_{max} applied to the stack converter is the design quantity through which the device thermal limit enters the analysis. The collapse limit V_c and the boundary of **Equation (4)** are properties of the power balance and are distinct from the undervoltage setting of the protection. V_c is the voltage at which the load-node equation loses its solution and lies far below any protection setting, whereas the boundary is a degradation level. The equilibrium bus voltage at the boundary, 857–873 V in **Table 5**, is 12.7 to 14.3 % below the nominal voltage of 1,000 V, and whether it lies within the allowable range is determined by the voltage tolerance and the undervoltage protection setting specified for each system; when the setting lies above this voltage, the protection rather than the power balance limits the step capability near the boundary. Because the decline that follows the crossing of the boundary is slow, an undervoltage protection set by the designer between the regulated range and V_c intervenes during the decline, and the time to collapse of Section 3.5 is the upper bound of the time within which that protection or a load-shedding action must act. The protection setting shortens the available time but does not move the boundary. The absolute times to collapse are properties of the modeled system; the trend with degradation and the scaling with capacitance follow from the structure of **Equations (4)** and **(5)** and are expected to hold for other systems of this class. The model is the appropriate instrument for this question because the degradation level is a slowly varying parameter that cannot be set on an installed system, whereas the model evaluates the boundary over the whole range of degradation and step size; a measurement on an installed system records one point of that plane and is complementary to the model-based evaluation.

For an actual shipboard system the quantities that enter **Equation (4)** are the feeder resistance, the stack sizing margin and the battery dispatch mode, and the boundary is evaluated with the values of that system. With the 1 mΩ feeder of Section 3.6, for instance, **Equation (4)** places the boundary for the 10 % step at 52 % ASR growth and those for the 3 and 5 % steps beyond 100 %, so that in a feeder of usual design the step size that becomes critical within the service life is of the order of 10 % rather than the 2 to 3 % of the reference feeder; the mechanism of the deferred collapse, the proportionality of its time to the bus capacitance and the shift of the boundary with battery participation are the same in both cases. The results therefore transfer to an installed system through this evaluation rather than through the numerical values of **Table 5**.

5. Conclusion

This study constructed an eleventh-order coupled dynamic model of the electrochemical states of an SOFC stack and the power conversion states of a shipboard DC distribution system, and quantified the effect of stack degradation on the load-following capability of a system with constant power loads. The principal results are as follows.

First, degradation directly erodes the stack current margin under constant power operation. A 50 % increase in ASR reduces the margin from 5.98 % to 0.08 %. The BoL current margin coincides numerically with the fractional stack voltage loss that can be tolerated, and this relation allows the design margin to be converted directly into a tolerable amount of degradation.

Second, small-signal eigenvalue analysis does not represent this risk. At 25 % ASR growth the damping ratio changes by only 0.2 % and the eigenvalues shift by at most 3.3 % while remaining stable,

whereas the stack current has already reached 96.8 % of the limit; the linearized model does not contain the current-limit inequality, so the distance to the limit cannot appear in its eigenvalues.

Third, the collapse boundary, defined by the existence of a saturated equilibrium in the full bus power balance, lies at 42.9, 29.5 and 16.1 % ASR growth for load steps of 1, 2 and 3 %, and predicts the outcome of all 45 transient cases. Beyond the boundary the bus voltage declines by discharge of the bus capacitance against a net current deficit of a few amperes, and the time to collapse follows from a quasi-static integral that reproduces the simulations within 7 % away from the boundary and is conservative near it, where the time extends to 4.06 s. The time scales with the bus capacitance, and battery droop participation shifts the boundary to the combined current headroom of stack and battery.

Fourth, at a reference degradation rate of 0.5 % per thousand hours the 2 % step capability is lost after 0.9 years while the static margin lasts 1.6 years. The service life of the stack in this system is therefore limited by load-following capability rather than by steady-state margin, and the boundary and time expressions provide the design basis for the bus capacitance and the battery regulation mode that preserve it.

The scope of the results is set by three choices. Degradation is represented by ASR growth, which is the quantity through which every mechanism of slow degradation enters the stack polarization; thermal cycling, seal degradation and abrupt failure modes act through other variables and are addressed by a competing-risk analysis **[11]**. The converters are described by averaged models, which is sufficient for the time scale of the collapse, as Section 4 discusses. The quantitative values refer to a battery dispatched at constant power behind a feeder dissipating 4.8 % of the load; the sensitivity cases of Section 3.6 show how the boundary moves with the battery regulation mode and the feeder design, and the extension to voyage load profiles and to probabilistic degradation parameters follows directly from the boundary and time expressions.

Appendix A. Model Parameters and State Equations

With the current density $j = i_{st}/A$ and the Nernst voltage $E(U_f)$, the eleven states obey the following equations, in which j_{BV} denotes the Butler–Volmer current density as a function of overpotential, $F_{fuel} = \min\{1, \max[0.25, i_{st}/I_r]\}$ the fuel-flow fraction, and g a gate equal to 1 outside saturation and 0 inside:

Table A1: Model parameters (reference condition)

Quantity	Symbol	Value
Cells in series / strings in parallel / modules	N_{ser}, N_{par}, N_{mod}	440 / 5 / 10
Active area per cell; total	A_{cell}; A	360 cm²; 18,000 cm²
Operating temperature	T	1,023 K
Rated current density; rated fuel utilization	j_r; $U_{f,r}$	0.45 A/cm²; 0.75
BoL ohmic and activation ASR	$R_{ohm,0}$; $R_{act,0}$	0.09654; 0.07790 Ω·cm²
BoL total ASR	ASR_0	0.1764 Ω·cm²
Limiting current densities (anode, cathode)	$j_{L,an}$; $j_{L,ca}$	27.33; 69.33 A/cm²
Transfer coefficients (anode, cathode)	α_{an}; α_{ca}	0.59; 0.65
Stack current limit	I_{max}	8,910 A (1.10 × rated)
Double-layer corner frequencies (anode, cathode)	–	1,899.6 Hz; 52.49 Hz
Gas-diffusion corner frequencies (anode, cathode)	–	0.33 Hz; 7.8 Hz
Fuel-utilization time constant	τ_{fuel}	0.50 s
Droop no-load setpoint; droop	V_{set}; K_{droop}	1,000 V; 5 % of 1,000 V per 5,000 A
Converter efficiency	η	0.98
Feeder resistance (60 m)	R_c	8.4 mΩ (1 mΩ in Section 3.6)
Propulsion CPL; hotel ZIP load	P_{CPL}; P_{ZIP}	4.0 MW; 1.0 MW (Z:I:P = 0.3:0.2:0.5)
Bus capacitance	C_{bus}	0.08 F (0.04 F in Section 3.5)
Voltage-loop gains (20 Hz, 60° phase margin)	K_p; K_i	10.05 A/V; 729.4 A/(V·s)
Current-loop bandwidth; drive bandwidth	ω_i; ω_{drive}	2π·200 Hz; 2π·100 Hz
Saturation smoothing width	w_{sat}	25 A
Battery open-circuit voltage (SOC 0.60)	V_{oc}	716.3 V
Battery series resistances	R_0; R_1; R_2	8.11; 2.72; 6.06 mΩ
Battery RC time constants	τ_1; τ_2	5.11 s; 66.0 s
Battery power setpoint; current limit	P_b; $I_{bt,max}$	2.0 MW; 3,360 A
Battery droop (Section 3.6); dead band	K_{batt}	78.8 kW/V (5 %); ±4 V

$$C_{dl,an}\, d\eta_{an}/dt = j - j_{BV}(\eta_{an};\, i_{0,an},\, \alpha_{an},\, 2)$$

$$C_{dl,ca}\, d\eta_{ca}/dt = j - j_{BV}(\eta_{ca};\, i_{0,ca},\, \alpha_{ca},\, 4)$$

$$\tau_{gd,an}\, d\eta_{agd}/dt = -(RT/2F)\, \ln(1 - j/j_{L,an}) - \eta_{agd}$$

$$\tau_{gd,ca}\, d\eta_{cgd}/dt = -(RT/4F)\, \ln(1 - j/j_{L,ca}) - \eta_{cgd}$$

$$\tau_{fuel}\, dU_f/dt = U_{f,r}\, (i_{st}/I_r) / F_{fuel}(i_{st}) - U_f$$

$$di_{st}/dt = \omega_i\, (i_{st,cmd} - i_{st}),\;\; i_{st,cmd} = \mathrm{sat}_{[0,\, Imax]}(v_S\, i_{out,cmd} / (\eta\, v_{st}))$$

$$i_{out,cmd} = K_p\, (v_{ref} - v_S) + K_i\, x_v,\;\; v_{ref} = V_{set} - K_{droop}\, i_{out,s}$$

$$\mathrm{d}x_v/\mathrm{d}t = (v_{\mathrm{ref}} - v_S)\, g$$

$$C_{\mathrm{bus}}\, \mathrm{d}v_S/\mathrm{d}t = i_{\mathrm{out,s}} + i_{\mathrm{out,b}} - i_c,\ \ i_{\mathrm{out,s}} = \eta\, v_{\mathrm{st}}\, i_{\mathrm{st}} / v_S,\ \ i_{\mathrm{out,b}} = \eta\, v_{\mathrm{bt}}\, i_{\mathrm{bt}} / v_S$$

$$C_1\, \mathrm{d}v_1/\mathrm{d}t = i_{\mathrm{bt}} - v_1/R_1,\ \ C_2\, \mathrm{d}v_2/\mathrm{d}t = i_{\mathrm{bt}} - v_2/R_2$$

$$\mathrm{d}P_{\mathrm{act}}/\mathrm{d}t = \omega_{\mathrm{drive}}\,(P_{\mathrm{CPL}} - P_{\mathrm{act}})$$

with $v_{\mathrm{st}} = N_{\mathrm{ser}}\,[E - j\,R_{\mathrm{ohm}} - \eta_{\mathrm{an}} - \eta_{\mathrm{ca}} - \eta_{\mathrm{agd}} - \eta_{\mathrm{cgd}}]$, $v_{\mathrm{bt}} = V_{\mathrm{oc}} - i_{\mathrm{bt}}\,R_0 - v_1 - v_2$, and the load node $(v_S - v_B)/R_c = P_{\mathrm{act}}/v_B + i_{\mathrm{ZIP}}(v_B)$. The saturation and the gate are smooth functions of width w_{sat}.

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Author Contributions

Conceptualization, E.-J. Park; Methodology, E.-J. Park; Software, H. Kwon and E.-J. Park; Validation, H. Kwon; Formal Analysis, H. Kwon; Investigation, H. Kwon; Resources, E.-J. Park; Data Curation, H. Kwon; Writing—Original Draft Preparation, H. Kwon; Writing—Review and Editing, E.-J. Park; Visualization, H. Kwon; Supervision, E.-J. Park; Project Administration, E.-J. Park.

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